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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/026,532	12/27/2001	Ryouichirou Nagamine	PNDF-01197	9433

7590 08/25/2004

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/026,532	NAGAMINE ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-7 is/are rejected.

7)☒ Claim(s) 2 and 4 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 27 December 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/27/01.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-7 are presented for examination.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on December 27, 2001 has been considered by the examiner. Form 1449 has been signed and returned with this office action.

Drawings

The drawings were received on December 27, 2001. These drawings are acceptable.

Specification

Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

The disclosure is objected to because of the following informalities:

35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with terms which are not clear, concise and exact. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification are:

33On page 2 lines 20-23 of the specification "In case that the test pattern is generated by using the scan path technique, a greater part of the test time is spent in a state that the signal is successively shifted on the scan path forming a shift register." Is unclear how a test pattern can be generated by "using the scan path technique" which would require the greater part of the test time... the examiner will assume for the purpose of examination, the second part of that sentence to mean: when the scan path is very long, it takes a significant amount of the testing time to shift the pattern through the entire scan path.

On page 3 lines 2-11, the paragraph has been understood to mean that the scan path is divided into multiple stages which have some physical relationship to the location of the input and output of the input and output terminals of the test circuit, for the purpose of examination.

On page 3 line 12, "convention" should be "conventional".

On page 3, lines 14, 17, 18, and 23, on page 4, line 26, and on page 5 line 7, the term "standing" in unclear with reference to the location of the FF's. In fact, the examiner is unclear what this term 'standing' is unless it is intended to be 'located'. Applicant is required to provide a clarification of these matters or correlation with art-accepted terminology so that a proper comparison with the prior art can be made.

On page 4, line 1, "in case" should be "in the case".

On page 4, line 20 the term 'issuer' should be issue.

On page 5, line 12 "connected with the left input terminal" is unclear

On page 5 line 26, "in case" should be "in the case".

Page 12 line 12 'ad' should be 'and'.

Although every error is not specifically pointed out, the specification should be checked or proofread to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The summary of invention on pages 6-11 appears to be a copy of the claims or parts of the claim language. The following is an excerpt from the MPEP:

608.01(d) Brief Summary of Invention

37 CFR 1.73. Summary of the invention

A brief summary of the invention indicating its nature and substance, which may include a statement of the object of the invention, should precede the detailed description. Such summary should, when set forth, be commensurate with the invention as claimed and any object recited should be that of the invention as claimed. Since the purpose of the brief summary of invention is to apprise the public, and more especially those interested in the particular art to which the invention relates, of the nature of the invention, the summary should be directed to the specific invention being claimed, in contradistinction to mere generalities which would be equally applicable to numerous preceding patents. That is, the subject matter of the invention should be described in one or more clear, concise sentences or paragraphs. Stereotyped general statements that would fit one application as well as another serve no useful purpose and may well be required to be canceled as surplusage, and, in the absence of any illuminating statement, replaced by statements that are directly on point as applicable exclusively to the case at hand.

The brief summary, if properly written to set out the exact nature, operation, and purpose of the invention, will be of material assistance in aiding ready understanding of the patent in future searches. The brief summary should be more than a mere statement of the objects of the invention, which statement is also permissible under 37 CFR 1.73. The brief summary of invention should be consistent with the subject matter of the claims.

Appropriate correction is required.

An amendment, which clarifies the disclosure so that the examiner may make a better comparison of the invention with the prior art is expected with the response to this office action. Applicant should be careful not to introduce any new matter into the disclosure (i.e., matter which is not supported by the

disclosure as originally filed).

Claim Objections

Claim 2 is objected to because of the following informalities: In line 1 of claim 2, "A test circuit for logical integrated circuit" should be "A test circuit for a logical integrated circuit". Appropriate correction is required.

Claim 4 is objected to because of the following informalities: In line 2 of claim 4, "is compose of" should be "is composed of". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, lines 6 and 7, "plural logic gates, output terminals of which are respectively connected with input terminals of said plural FFs", it is unclear from the claims and the specification what the function of 'plural logic gates' is intended to be. These logic gates could be another flip-flop, or any type of functional logic block (however this is not clearly disclosed in the specification). For purpose of examination the examiner will assume the plural logic gates to be an output from a functional block of internal circuitry to be tested.

In lines 13-14, "wherein said scan path connects an output terminal of said FF standing at an end of said first stage with a scan output" is unclear.

In lines 13 and 14 'said FF' is unclear as previous reference to FF is plural.

As per claim 2, lines 5 and 6, "plural logic gates, output terminals of which are respectively connected with input terminals of said plural FFs", it is unclear from the claims and the specification what the function of 'plural logic gates' is intended to be. These logic gates could be another flip-flop, or any type of functional logic block (however this is not clearly disclosed in the specification). For purpose of examination the examiner will assume the plural logic gates to be an output from a functional block of internal circuitry to be tested.

In line 12, "said FF standing at a head of said n th stage" is unclear.

In line 12 'said FF' is unclear as previous reference to FF is plural.

As per claim 3, lines 5 and 6, "plural logic gates, output terminals of which are respectively connected with input terminals of said plural FFs", it is unclear from the claims and the specification what the function of 'plural logic gates' is intended to be. These logic gates could be another flip-flop, or any type of functional logic block (however this is not clearly disclosed in the specification). For purpose of examination the examiner will assume the plural logic gates to be an output from a functional block of internal circuitry to be tested.

In lines 12-21, "wherein said scan path connects a scan input with an input terminal of *said FF* standing at a head of said n th stage, again successively connects said FFs arranged in said second to (n-1) th stages in series, after *restarting* from an output terminal *said FF* standing at an end of said n th stage, once again connects an output terminal of *said FF* standing at an end of said (n-1) th stage with an input terminal of *said FF* standing at a head of said first stage, and finally connects an output terminal of *said FF* standing at an end of said first stage with a scan output." The terms underlined above, with the "said FF standing..." is unclear. Also, the terms 'said FF' in italics and underlined above, do not appear to be referring to an individual FF although it is referenced in the singular and previous references are to FFs in a plural form. The term "restarted' in italics above, is unclear as there is no indication as to an initial start or stop. Claim 3 is so unclear that it will not be further treated on the merits.

As per claim 4, lines 5 and 6, "plural logic gates, output terminals of which are respectively connected with input terminals of said plural FFs", it is unclear from the claims and the specification what the function of 'plural logic gates' is intended to be. These logic gates could be another flip-flop, or any type of functional logic block (however this is not clearly disclosed in the specification). For purpose of examination the examiner will assume the plural logic gates to be an output from a functional block of internal circuitry to be tested.

In line 12 "said FF" standing at an end" is unclear.

In line 12 'said FF' is unclear as previous reference to FF is plural.

As per claim 5, lines 5 and 6, "plural logic gates, output terminals of which are respectively connected with input terminals of said plural FFs", it is unclear from the claims and the specification what the function of 'plural logic gates' is intended to be. These logic gates could be another flip-flop, or any type of functional logic block (however this is not clearly disclosed in the specification). For purpose of examination the examiner will assume the plural logic gates to be an output from a functional block of internal circuitry to be tested.

In lines 12 and 13, "said FF standing at a head" is unclear.

In line 12, 'said FF' is unclear as previous reference to FF is plural.

As per claim 6, lines 5 and 6, "plural logic gates, output terminals of which are respectively connected with input terminals of said plural FFs", it is unclear from the claims and the specification what the function of 'plural logic gates' is intended to be. These logic gates could be another flip-flop, or any type of functional logic block (however this is not clearly disclosed in the specification). For purpose of examination the examiner will assume the plural logic gates to be an output from a functional block of internal circuitry to be tested.

In lines 12-21, "connecting a scan input with an input terminal of *said FF* standing a head of said n th stage, connecting said FFS arranged in said second to (n-1) th stages successively in series, after *restarting* from an output terminal of *said FF* standing at an end of said n th stage, connecting an output terminal of *said FF* standing at an end of said (n-1) th stage with an input terminal of *said FF*

standing at a head of said first stage, connecting an output terminal of *said FF* standing at an end of said first stage with a scan output,". The terms underlined above, with the "said FF standing..." is unclear. Also, the terms 'said FF' in italics and underlined above, do not appear to be referring to an individual FF although it is referenced in the singular and previous references are to FFs in a plural form. The term "restarted' in italics above, is unclear as there is no indication as to an initial start or stop. Claim 6 is so unclear that it will not be further treated on the merits.

As per claim 7, lines 5 and 6, "plural logic gates, output terminals of which are respectively connected with input terminals of said plural FFs", it is unclear from the claims and the specification what the function of 'plural logic gates' is intended to be. These logic gates could be another flip-flop, or any type of functional logic block output (however this is not clearly disclosed in the specification). For purpose of examination the examiner will assume the plural logic gates to be an output from a functional block of internal circuitry to be tested.

In lines 12-20, "connecting a scan input with an input terminal of *said FF* standing a head of said n th stage, connecting said FFs arranged in said second to (n-1) th stages successively in series, after *restarting* from an output terminal *said FF* standing at an end of said n th stage, connecting an output terminal of *said FF* standing at an end of said (n-1) th stage with an input terminal of *said FF* standing at a head of said first stage, connecting an output terminal of *said FF*

standing at an end". The terms underlined above, with the "said FF standing..." is unclear. Also, the terms 'said FF' in italics and underlined above, do not appear to be referring to an individual FF although it is referenced in the singular and previous references are to FFs in a plural form. The term "restarted' in italics above, is unclear as there is no indication as to an initial start or stop. Claim 7 is so unclear that it will not be further treated on the merits.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2 and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Whetsel U. S. Patent No. 6,199,182.

As per claims 1 and 2, Whetsel teaches that scan testing of circuits is well known. Scan testing configures the circuit into scan cells and combinational logic. Once so configured, the scan cells are controlled to capture test response data from the combinational logic, then shifted to unload the captured test response data from the combinational logic and to load the next test stimulus data to apply to the combinational logic. Also, in FIG. 39A, the tester includes a

conventional scan interface for controlling scan operations, signal generators for producing DC and AC test signals, voltmeters for measuring DC and AC voltages, a first switching circuit (SW1) for connecting the tester's TSA or TSB terminals to the voltmeter or signal generators, a second switch circuit (SW2) for connecting the tester's TSC terminal, through a known resistor R, to a programmable voltage source (Vp), and a conventional test control computer for controlling the overall operation of the tester. (Figure 39A, column 1 lines 18-24, column 20 lines 4-13)

As per claims 4 and 5, Whetsel teaches that scan testing of circuits is well known. Scan testing configures the circuit into scan cells and combinational logic. Once so configured, the scan cells are controlled to capture test response data from the combinational logic, then shifted to unload the captured test response data from the combinational logic and to load the next test stimulus data to apply to the combinational logic. Also, in FIG. 39A, the tester includes a conventional scan interface for controlling scan operations, signal generators for producing DC and AC test signals, voltmeters for measuring DC and AC voltages, a first switching circuit (SW1) for connecting the tester's TSA or TSB terminals to the voltmeter or signal generators, a second switch circuit (SW2) for connecting the tester's TSC terminal, through a known resistor R, to a programmable voltage source (Vp), and a conventional test control computer for controlling the overall operation of the tester. FIG. 1 shows an electrical circuit having three memories (M) A, B, C and combinational logic (CL). FIG. 2 shows

an example of the memories of FIG. 1 implemented as D flip-flops (FF), each memory having a data input, data output, and clock and reset control signals. FIG. 3 shows one example of how the circuit of FIG. 1 can be made scan testable by converting the memories into scan cells and connecting the outputs (D, E, F) of the combinational logic to the scan cell capture inputs. FIG. 4A shows an example of how a D flip flop based memory is converted into a scan cell. The scan cells have a 3:1 multiplexer input to the flip-flop. The multiplexer receives selection control (S) to: (1) input the output of the combinational logic to the flip flop (Input1, the capture input), (2) input the external input to the flip flop (Input2, the functional input), or (3) input the serial input to the flip-flop (SI, the shift input). The flip-flop receives a clock (C) and a reset (R) control input. The scan cells are connected together via their serial input (SI) and serial output (SO) to form a 3-bit scan path through the circuit of FIG. 3. The three scan cells operate as the state memories during functional operation. During test operation, the scan cells operate as scan cells to allow inputting test stimulus to the combinational logic and capturing the response output from the combinational logic. While edge sensitive D flip-flop memories are used in this disclosure, level sensitive memories could be used as well. (Figures 1-4 and 39A, column 1 lines 18-50, column 20 lines 4-13)

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,544,173 Meltzer

This patent teaches scan testing of complex electronic logic circuits for the detection of AC delay faults is improved without the addition of dummy or test-only latches by connecting the shift register latches according to the order determined by the method of first listing all shift register latches in the scan chain with all the combinational circuit outputs traceable from the output; sorting this list in the order of number of outputs controlled, i.e., touched in the forward trace; listing each unique combinational circuit output; sequentially assigning the order of the SRLs in the scan chain so that adjacent SRLs do not control any of the same circuit outputs; when this is not possible assign adjacent SRLs so that the fewest common circuit outputs are controlled by adjacent SRLs or if any remain unassigned, insert an output SRL between adjacent SRLs.

U.S. Patent No. 6,343,365 Matsuzawa et al.

This patent teaches that in a large-scale integrated circuit, a scan path is divided between an I/O scan path that is formed by a series connection between only flip-flops that are in a region near an I/O pin and an internal scan path that is formed by a series connection between other flip-flops. A selector has one of its inputs connected to another end of the I/O scan path and to one end of the internal scan path, another of its inputs connected to another end of the internal scan path, and its output connected to a scan out. This selector, based on a test mode signal, selects either all scan paths or only the I/O scan path.

U.S. Patent No. 6,574,760 Mydill

This patent teaches an automatic test apparatus for assuring quality and reliability of semiconductor integrated circuit devices comprising a computerized tester controller performing virtual timing, formatting, and pattern generation for testing said devices; and a test head controlled by the controller, comprising pin electronics, dc subsystem, and support for self-testing built into the circuit. The computerized tester controller comprises pattern sequence control, pattern memory, scan memory, timing system and driver signal formatter, thereby executing virtually high speed functional tests based on test patterns, combined with ac parametric tests of said devices.

TW 413981A Jeng et al.

This patent teaches two new analog boundary scan designs for testing and diagnosing analog or mixed-mode circuits. The basic analog boundary scan cell, the defined instructions with the associated operations, and the control circuitry of each design are described. The advantages of these two designs include: (1) Signal at various test points can be sampled simultaneously; (2) test stimuli can be injected to various test points simultaneously and (3) test stimuli loading and test response outputting can be done simultaneously. The first design is for DC testing while the second design can be used for both DC and AC testing.

JP02000097997A Teramoto, Hiroyuki

This patent teaches an LSI device with a function of boundary scan tests with both an interface circuit between an internal circuit and a boundary scan register and a control circuit to receive a signal obtained by decoding a personal command for executing AC measurement on device input pins and device output pins by a command decoder and to output a control signal. By this, it is possible to observe from the device input pins to a first-stage flop-flop and from a final-stage flip-flop to the device output pins.

JP404050783A Koumae Seiichi

This patent teaches in order to shorten a test time and to inspect Ac characteristics by fetching scan-out data of an LSI in a following stage in synchronism with a clock and transferring it to a precedent stage when a scan-path data (SPD) return mode is selected.

"IDDQ and AC Scan: The War Against Unmodelled Defects" by Maxwell et al. International Test Conference Proceedings Publication Date: 20-25 Oct. 1996 pages 250 - 258 Inspec Accession Number: 5539851

This paper investigates the relative effectiveness of scan-based AC tests, IDDQ tests and functional tests for the detection of defective chips, particularly those exhibiting delay faults. Data are presented from an experiment in which a production ASIC was tested with a number of scan and functional tests, together with IDDQ. Results show that all tests detect unique failures, indicating the presence of additional unmodelled faults. The effectiveness of the AC tests

shows that targeting additional faults produces better quality than relying on peripheral coverage of existing tests

"The Testability Features of the 3rd Generation ColdFire(R) Family of Microprocessors" by Crouch et al. International Test Conference Proceedings Publication Date: 28-30 Sept. 1999 pages 913 - 922 Inspec Accession Number: 6536446

This paper gives a description of the DFT and test challenges faced, and the solutions applied, to the newest member of the ColdFire(R) microprocessor family. The MCF5307 is the first member of the family to have on-chip, PLL-sourced, dual clock domains where the bus interface and the internal core microprocessor operate at different, but selectable, frequency ratios; and the internal microprocessor core of the MCF5307 was designed as a separate stand-alone core that contained multiple embedded memory arrays. The DFT challenges and solutions described involve the development of the at-speed AC scan test architecture and scan vectors in a multiple clock domain environment; the application of memory BIST to multiple embedded memories in a cost effective manner; and the handling of an on-chip PLL clock

"Analogue Boundary Scan Architecture for DC and AC Testing" by Kuen-Jong Lee et al. Electronics Letters Publication Date: 11 April 1996 pages 704 - 705 Volume: 32, Issue: 8 Inspec Accession Number: 5251377

This paper teaches a new mixed-mode boundary scan architecture that is developed. The digital part of this architecture complies with the IEEE Standard 1149.1. For the analogue part, we propose a new boundary scan cell design and define four analogue test instructions. The control signals for each instruction are also described.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100